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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,787	12/02/2003	Michael J. Koster	SUN-P8985-SPL	6112

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EXAMINER	
THOMAS, SHANE M	
ART UNIT	PAPER NUMBER
2186	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/726,787	KOSTER ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,7-10 and 16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7-10 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.1 14, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.1 14, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/2/2006 has been entered.

All previously outstanding objections and rejections to the Applicant's disclosure and claims not contained in this Action have been respectfully withdrawn by the Examiner hereto.

Response to Amendment/Arguments

Applicant has amended independent claims 1,10,19, and 20, to incorporate the limitations of (1) monitoring the dynamic behavior of the cache on a cache line by cache line basis; (2) switching from a write-broadcast to a write-invalidate protocol if the particular cache line is not contended for frequently by multiple processors; and (3) the switching being performed by a cache controller in the processor.

The Examiner has modified the previous rejection to incorporate the prior art reference of Ivosevic et al., which teaches a methodology for switching between a write-update protocol (synonymous with write-broadcast) when the contention (number of writes to a line) by multiple processors falls below a threshold (page 42, column 1, paragraph 5). Refer to the rejections below.

Applicant's amendment to the claims has given rise to a 35 U.S.C. §112, second paragraph, rejection as well for not particularly pointing out and distinctly claiming the subject matter of the invention.

Applicant arguments presented in the response filed 10/02/2006 have been rendered moot by the newly presented rejections below.

Claims

The Examiner notes Applicant's use of conditional limitations within the claims. As discussed in MPEP ¶2111.04, as the limitations of (1) switching the cache protocol from a write-invalidate to write-broadcast if the behavior indicates better performance can be achieved and (2) switching the cache protocol back to write-invalidate are made optimal by the use of "if" language. Therefore, a prior art reference that merely comprises a caching system initialized to a write-invalidation protocol - even a system that never uses a write-broadcast protocol - that also monitors the cache lines for the dynamic behavior of a number of invalidations would adequately teach the invention as claimed. If the Applicant's desire is to limit the claims to incorporate the limitations that are currently deemed optional, the Examiner recommends merely amending the conditional terms "if" (e.g. lines 11 and 15 of claim 1, for example) to "when." Such an amendment clearly indicates an implication that at some point in time, during the operation of the system/method claimed, the condition will be met and the limitation realized.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 7-10, and 16-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1,10,19, and 20, it is not clear whether the term --the count for the cache line number of cache line updates-- is the same as the previously defined term --a count for maintaining a count of cache line invalidations-- or whether the term is a second count, specifically for the number of updates to a cache line, as the term --the count for the cache line number of cache line updates-- lacks antecedent basis. Regarding claim 20, --a count-- has not been previously defined in the claim, and therefore the term --the count for the cache line number of cache line updated-- lacks antecedent basis. Nonetheless, for the purposes of examination, the Examiner has considered the aforementioned term to be a count, separate from the count for invalidations, for the number of updates for a given cache line.

Claims 7-9 and 16-18 are rejected as being dependent upon a rejected basis claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 7-10, and 16-20, are rejected under 35 U.S.C. 102(e) as being unpatentable over Ang (U.S. Patent Application Publication No. 2003/0079085) in view of Ivosevic et al. ("Time Domain Performance Evaluation of Adaptive Hybrid Cache Coherence Protocols").

As per claims 1,10, and 20, Ang teaches **initializing a cache to operate using a write-invalidate protocol** (¶20), **monitoring a dynamic behavior of the cache during program execution** (¶65), **wherein monitoring the dynamic behavior of the cache involves monitoring the dynamic behavior of the cache on a cache line by cache line basis** (¶48 - invalidation and re-fetching frequencies are maintained for each cache line) **by maintaining a count for each cache line of the number of cache line invalidations the cache line has been subject to during program execution and if the dynamic behavior indicated that better performance can be achieved using a wrote-broadcast protocol, switching the cache to operate using the write-broadcast protocol** (¶48). In ¶48, Ang teaches when deciding to transition from the invalidation to the update protocol, which is known in the art to be synonymous with the write-broadcast protocol (¶3), the memory-side coherence engine tracks the frequency (i.e. the number of occurrences, thereby which a counter is inherent) of cache-line invalidations. When the frequency of the invalidations reaches a threshold, the cache coherence

protocol is dynamically switched from a write-invalidation scheme to a write-update (or write-broadcast) scheme.

Ang teaches in ¶48 that if no usage for a given cache line occurs over the span of a number if updates, the side-cache engine purges or removes the cache line from the cache. Once the memory-side coherence engine notices that all cache copies other than its own copy are purged, the policy of the cache line changes from a write-broadcast to a write-invalidate. Thus, Ang does not specifically teach **changing the policy to a write-invalidate based on the number of updates to the cache line indicating that the cache line is no being contended for frequently by the multiple processors.**

Ivosevic teaches on page 42, column 1, paragraph 5, that a count is maintained for the updates written by multiple processors to the specific cache line, and if the number of consecutive updates surpasses a threshold, a switch from write-update (e.g. write-broadcast) to write-invalidate occurs. The surpassing of the threshold can therefore be seen as the **cache line not being contented for frequently by multiple processors** as only a single processor is accessing the cache line. Further, the Examiner could interpret the contention of the cache line by multiple processors to be the read access by the other processors of the cache line when updated. Under this interpretation, Ivosevic further teaches on page 42, column 2, paragraphs 1-2, that read accesses may contribute to the threshold determination regarding whether or not a switch from write-update to write-invalidate should occur.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the cache system of Ang with the write-broadcast to

write-invalidation teaching of Ivosevic in order to have reduced bus traffic when only a single processor accesses the cache line (page 42, column 2, paragraph 2).

As discussed in the Response to Amendments section of the Final Office action filed 9/7/2006, the steps of **initializing, monitoring and switching** may be **performed by the cache controller in the processor** 102 (¶¶61-63 of Ang).

As per claims 7 and 16, modified Ang does not specifically teach **wherein if a shared memory multiprocessor includes modules that are not able to switch to the write-broadcast protocol, locking the cache into the write-invalidate protocol**; however, such a limitation would have been obvious to one having ordinary skill in the art at the time the invention was made, as a given processor operating in the write-invalidate mode amongst other processors of a shared memory multiprocessor system operating in a write-update mode would pose a data integrity issue. Such obviousness is best set forth via an example. If cache line address A is currently shared among a first processor operating in a write-broadcast mode a second processor in a write-invalidate mode and the first processor modified address A, the first processor would also send out the updated data associated with address A (as discussed in the write-update protocol definition in Ang ¶3 and Applicant's ¶9). The second processor, not operating in the write-update mode would never receive the updated data (as it only awaits for invalidation messages to notify of shared cache line modifications) and instead assumes the data associated with address A contained within its local cache is still valid. Therefore, when the second processor attempts to read from its local cache line address A, the data, as appears to the shared memory, is invalid as the first processor had already updated this data. Thus the data read by processor from its local cache would have been invalid.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have further modified the cache coherency protocol of Ang to have locked the multiprocessor caches into a write-invalidate mode, if the cache (or portion thereof) of a particular processor of the multiprocessor shared memory system was not capable of switching to a write-broadcast protocol, thereby maintaining data integrity by way of keeping the caching policies among the plurality of processors in the multiprocessor shared memory system coherent with each other.

As per claims 8 and 17, Ang teaches **the** [processor implementing a] **write-invalidate protocol sends an invalidation message to other caches in a shared memory multiprocessor when a given cache line is updated in a local cache** (¶20). Further the Applicant's Admitted Prior Art (herein "APA") teaches that such a limitation is inherent in write-invalidation protocols (¶6 of Applicant's specification).

As per claims 9 and 18, Ang teaches **the** [processor implementing a] **write-broadcast protocol broadcasts an update to other caches in a shared memory multiprocessor when the given cache line is updated in a local cache** (¶3). Further, the APA teaches that such a limitation is inherent in write-broadcast (i.e. write-updating) protocols (¶9).

As per claim 19, the rejection follows the rejection for claims 1, 10, and 20 set forth above. Further, Ang teaches **a plurality of processors** (abstract, and labeled 102 in figure 1), **wherein a processor within the plurality of processors includes a cache** 122, **a shared memory** 108, and **a bus** (connection shown in figure 1 between the network and between controller 106 of the node to the shared memory 108) **coupled between the plurality of processors and the shared memory, wherein the bus transports addresses and data between**

the shared memory and the plurality of processor (necessarily inherent in the system of Ang as it is well known in the art that in order to access a location in a memory, an address is required and in order to receive requested data, the data must be retrieved from the memory and sent back to the requesting processor/hardware unit).

As discussed in the Response to Amendments section of the Final Office action filed 9/7/2006, the steps of **initializing, monitoring and switching** may be **performed by the cache controller in the processor** 102 (¶¶61-63 of Ang).

Conclusion

Abily et al. (U.S. Patent No. 6,240,491) teaches a cache coherency policy for switching between an update and an invalidate mode for each cache block.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M. Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M. Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane M. Thomas

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